

Amendments to the Specification:

Please replace the **Title** with the following amended Title:

NON-VOLATILE MEMORY CELL WITH MULTI-POLYSILICON LAYERS GATES
STRUCTURE AND METHOD OF FORMING SAME

Please delete paragraphs **[09]**, and **[10]**.

Please replace paragraphs **[11]** and **[12]** with the following amended paragraphs:

[11] In another accordance with an embodiment of the present invention, a semiconductor non-volatile memory cell includes a first insulating layer over a substrate region. A floating gate includes a first polysilicon layer over the first insulating layer and a second polysilicon layer over and in contact with the first polysilicon layer. The first polysilicon layer has a predetermined doping concentration and the second polysilicon layer has a doping concentration which decreases in a direction away from an interface between the first and second polysilicon layers. A second insulating layer overlies and is in contact with the second polysilicon layer. A control gate includes a third polysilicon layer over and in contact with the second insulating layer, and a fourth polysilicon layer over and in contact with the third polysilicon layer. The fourth polysilicon layer has a predetermined doping concentration, and the third polysilicon layer has a doping concentration which decreases in a direction away from an interface between the third and fourth polysilicon layers. A first doped polysilicon layer overlies the first insulating layer, and a first undoped polysilicon layer overlies and is in contact with the first doped polysilicon layer. The doped and undoped polysilicon layers form a floating gate. A second insulating layer overlies and is in contact with the first undoped polysilicon layer. A second undoped polysilicon layer overlies and is in contact with the second insulating layer. A second doped polysilicon layer overlies and is in contact with the second undoped polysilicon layer. The second doped and undoped polysilicon layers form a control gate.

[12] In another embodiment, the memory cell floating gate further includes a third undoped fifth polysilicon layer over and in contact with the first insulating layer. The first doped polysilicon layer overlies and is in contact with the third undoped fifth polysilicon layer. The fifth polysilicon layer having a doping concentration which decreases in a direction away from an interface between the first and fifth polysilicon layers. The third undoped polysilicon layer forms part of the floating gate.

Please delete paragraphs [13], [14], and [15].

Appl. No. 09/994,545
Amdt. dated June 22, 2004
Response to Notice of Allowance April 22, 2004

PATENT

Amendments to the Drawings:

The attached six (6) replacement sheets of drawings include no changes to the Figures. These formal drawings are submitted as replacement sheets, to be made of record in the application.

Attachment: Replacement Sheets (6)